ADM-VPX3-9Z5-RTM
User Manual

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1 Introduction

The ADM-VPX3-9Z5-RTM is a 3U, VPX, Rear Transition Module (RTM) designed to interface with Alpha Data ADM-VPX3-9Z5 Zynq Ultrascale+ FPGA board.

The ADM-VPX3-9Z5-RTM provides complete breakout of all backplane signals providing the user with complete flexibility during development and debug.

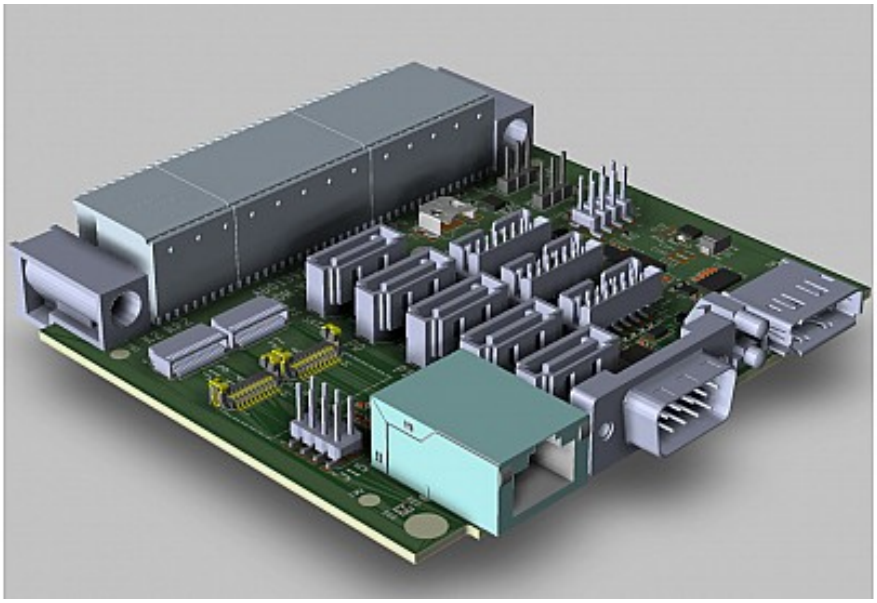

Figure 1 : ADM-VPX3-9Z5-RTM

1.1 Key Features

PS GTR IO

- IO Connectors from the GTR lanes from the PS side of the ADM-VPX3-9Z5:
  - One Gigabit Ethernet RJ45 port, available on the front panel
  - 1 SATA interface, via an internal standard connector
  - 1 DisplayPort interface, 2 lanes wide, available via the front panel
- 1 Serial COM port interfaces, available on the front panel
- 1 Serial CAN BUS interfaces, available on an internal header
- RTC Battery connection header
- GPIOs routed to an internal header which can be looped back via jumper links (for internal testing).
- 12 HSSIO differential pairs - connected to GTH lanes on the PL side of the ADM-VPX3-9Z5:
  - Two Firefly connectors (8 HSSIO pairs)
  - 4 SATA interfaces, via internal standard connectors (4 HSSIO pairs)
- Xilinx JTAG programming header

1.2 References & Specifications

ANSI/VITA 46.0	*VPX Baseline Standard*, October 2007, VITA, ISBN 1-885731-44-2
ad_ug_1341	*ADM-VPX3-9Z5 User Manual*, June 2021, Alpha Data, -

Table 1 : References

2 Installation

2.1 Software Installation

Please refer to the ADM-VPX3-9Z5 area on the Alpha-Data support site for access to system monitoring utilities, documentation and FPGA reference designs.

2.2 Hardware Installation

2.2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

3 Functional Description

3.1 Block Diagram

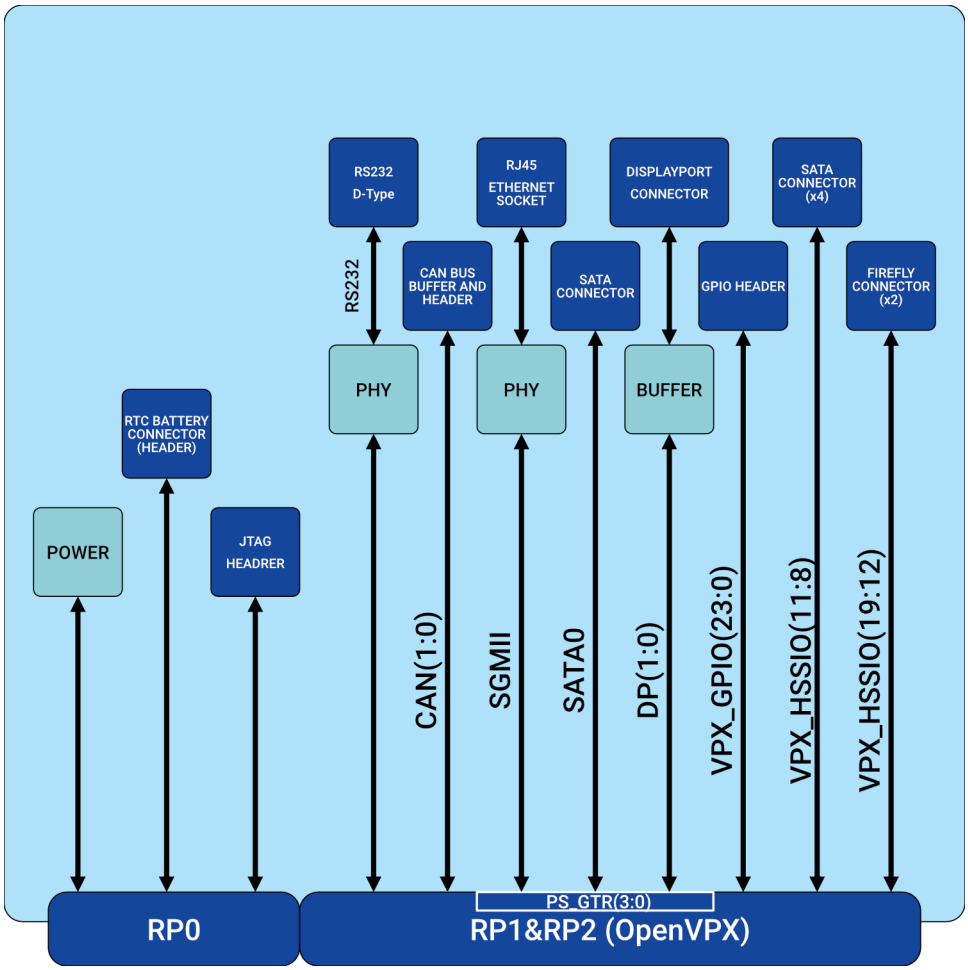

Figure 2 : ADM-VPX3-9Z5-RTM Block Diagram

3.2 Assembly Drawing

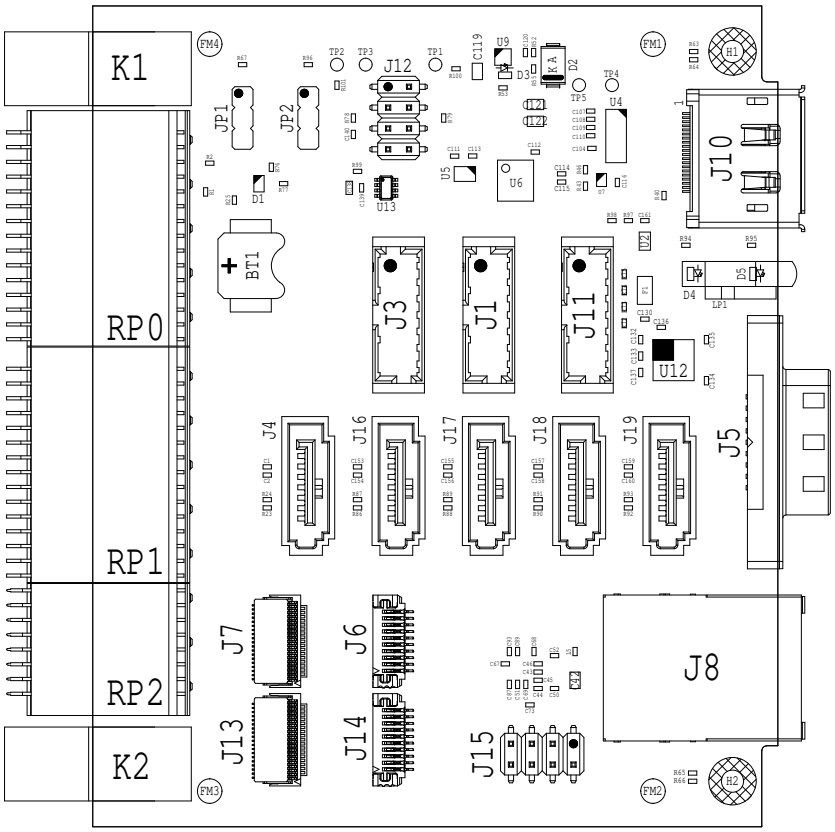

Figure 3 : ADM-VPX3-9Z5-RTM Top View

3.3 Connector Definitions

The description of the connectors on the board status shown below:

Comp. Ref.	Function
JP1	NVMRO - not required on ADM-VPX3-9Z5
JP2	GPIO Enable. position 1-2 = GPIO Headers Disabled : 2-3 = Enabled
J12	CANBUS Header
J10	DisplayPort Connector
BT1	RTC Battery Holder
J1+J3	GPIO Headers
J11	Xilinx Programming cable Connector
J4	PS side SATA interface
J16-J19	PL side SATA connectors
J5	RS232 Serial Port
J6-J7	Firefly Connector 0
J13-J14	Firefly Connector 1
J8	Ethernet
J15	GPIO Header

Table 2 : Connector Definitions

3.4 LED Definitions

The position and description of the board status LED is shown in LED Locations:

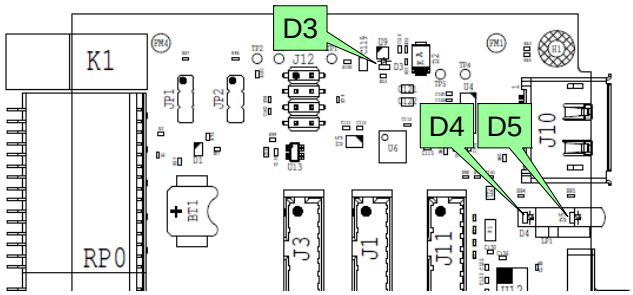

Figure 4 : LED Locations

Comp. Ref.	Function	ON State	Off State
D3(Green)	Display Port 3.3V Supply Status	Normal operation	Fault
D4(Green)	PSMIO31 LED	PSMIO=Logic Low	PSMIO=Logic High
D5(Green)	3.3V Supply Status	Normal operation	Power Off

Table 3 : LED Definitions

3.5 JTAG Interface

3.5.1 On-board Interface

The JTAG boundary scan chain can be accessed via a standard header (J11).

This allows the connection of the Xilinx JTAG cable for FPGA debug and Flash programming via the Xilinx toolchain.

3.5.2 JTAG Voltages

The Vcc supply provided to the JTAG cable on the config header is +3.3V and is protected by a poly fuse rated at 350mA.

3.6 HS MIO Interfaces

The ADM-VPX3-9Z5-RTM allows support for the following PS GTR interfaces: displayport, ethernet and SATA.

In order for the interfaces to be routed out correctly The PS GTR serial interfaces should be configured as highlighted in the table below:

Controller	PHY Lane 0	PHY Lane 1	PHY Lane 2	PHY Lane 3
PCIe v2.0	PCIe.0	PCIe.1	PCIe.2	PCIe.3
SATA	SATA.0	SATA.1	SATA.0	SATA.1
USB0 3.0	USB0	USB0	USB0	
USB1 3.0				USB1
DisplayPort	DP.1	DP.0	DP.1	DP.0
GEM0	GEM0			
GEM1		GEM1		
GEM2			GEM2	
GEM3				GEM3

Figure 5 : HS-MIO Configuration

3.7 Ethernet Phy Interface Signals

The reset_n pin of the Ethernet Phy is connected directly to the VPX system reset.

The Ethernet Phy MDIO BUS interface should be configured as shown in the table below:

Signal Name	FPGA Pin
MDC	PSMIO76 (AH31)
MDIO	PSMIO77 (AG31)

Table 4 : MDIO pins

3.8 Display Port AUX signals

The Display Port AUX interface should be configured as shown in the table below:

Signal Name	FPGA Pin
DP_AUX_OUT	PSMIO34 (P27)
DP_HPD	PSMIO35 (N29)
DP_OE	PSMIO36 (T27)
DP_AUX_IN	PSMIO37 (N30)

Table 5 : DPAUX pins

3.9 SATA Connectors

The ADM-VPX3-9Z5-RTM board has five standard right angle SATA receptacles for use with SATA compliant storage devices.

One of the SATA devices is connected to the PS side and the remainder are connected to the PL side.

Connector	Signal	FPGA Bank	"P" pin	"N" pin
PS_SATA (J4)	PS_TX0	PS Bank 505	AH39	AH40
	PS_RX0	PS Bank 505	AG41	AG42
PL_SATA0 (J16)	DP2_C2M	MGT Quad 226	AL6	AL5
	DP2_M2C	MGT Quad 226	AM4	AM3
PL_SATA1 (J17)	DP3_C2M	MGT Quad 226	AK8	AK7
	DP3_M2C	MGT Quad 226	AL2	AL1
PL_SATA2 (J18)	DP2_C2M	MGT Quad 226	AJ6	AJ5
	DP2_M2C	MGT Quad 226	AK4	AK3
PL_SATA3 (J19)	DP3_C2M	MGT Quad 226	AH8	AH7
	DP3_M2C	MGT Quad 226	AJ2	AJ1

Table 6 : SATA Connections

3.10 FireFly Connectors

Connector	Ref Des	FPGA Bank
0	J6-J7	MGT Quad 227
1	J13-J14	MGT Quad 228

Table 7 : Firefly Connectors

3.11 CAN BUS Header

The CAN BUS interface should be configured to PSMIO40/PSMIO41 (pins P28/P30) on the PS side of the FPGA on the ADM-VPX3-9Z5 board.

Pin	Signal Name
1	GND
2	GND
3	CAN_GND
4	CAN_H
5	CAN_L
6	CAN_GND
7	CAN_L
8	CAN_H

Table 8 : Header J12

3.12 RS232 Dtype

Pin	Signal Name	FPGA Pin
1	-	-
2	TXD	PSMIO39 (P29)
3	RXD	PSMIO38 (R27)
4	-	-
5	GND	-
6	-	-
7	-	-
8	-	-
9	-	-

Table 9 : Header J5

3.13 GPIO Headers

Pin	Signal Name	FPGA Pin
1	P1_GP_1V8_P_10	AU11
2	P1_GP_1V8_P_9	AW11
3	P1_GP_1V8_N_10	AV11
4	P1_GP_1V8_N_9	AW10
5	GP4_1V8_P	AJ15
6	GP3_1V8_P	AM13
7	GP4_1V8_N	AK15
8	GP3_1V8_N	AN13
9	GP2_1V8_P	AN14
10	GP1_1V8_P	AJ14
11	GP2_1V8_N	AP14
12	GP1_1V8_N	AK14

Table 10 : Header J1

Pin	Signal Name	FPGA Pin
1	P1_GP_1V8_P_12	BB5
2	P1_GP_1V8_P_11	AV12
3	P1_GP_1V8_N_12	BB4
4	P1_GP_1V8_N_11	AW12
5	GP8_1V8_P	AM11
6	GP7_1V8_P	AM10
7	GP8_1V8_N	AN11
8	GP7_1V8_N	AN10
9	GP6_1V8_P	AL15
10	GP5_1V8_P	AL14
11	GP6_1V8_N	AM15
12	GP5_1V8_N	AM14

Table 11 : Header J2

Pin	Signal Name	FPGA Pin
1	GP_SE_3V3_5	D2
2	GP_SE_3V3_2	C3
3	GP_SE_3V3_4	C5
4	GP_SE_3V3_3	C6
5	GP_SE_3V3_6	C1
6	GP_SE_3V3_1	C4
7	GP_SE_3V3_7	D4
8	GP_SE_3V3_0	B1

Table 12 : Header J15

Revision History

Date	Revision	Nature of Change
08 June 2021	1.0	Initial Release
18 August 2022	1.1	Added extra detail to tables

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